## WHAT IS CLAIMED IS:

- 1. A method for forming an MIM capacitor of a semiconductor  $\square$ device, the method comprising the steps of:
- 5 i) forming a via at a first insulating layer in order to expose a lower metal wire;
  - ii) forming a first barrier layer at a surface of the first insulating layer including the via;
- iii) forming a metal layer on the first insulating layer

  in which the first barrier layer is formed;
  - iv) forming a capacitor lower electrode layer after
    forming a second barrier layer and a third barrier layer on
    the metal layer;
- v) forming a dielectric layer by oxidizing the capacitor 15 lower electrode layer;
  - vi) forming a capacitor upper electrode layer on the dielectric layer; and
- vii) patterning the capacitor upper electrode layer, the dielectric layer, and the capacitor lower electrode layer, 20 thereby forming the capacitor.
  - 2. The method according to claim 1, wherein the capacitor lower electrode layer is formed using a metal capable of forming a layer having high dielectric constant.

- 3. The method according to claim 2, wherein the metal is formed with an amorphous structure by using one process selected from the group consisting of CVD, ALD and sputtering processes.
- 4. The method according to claim 2 or 3, wherein the metal is one selected from the group consisting of TaN, Ta, Ti, TiN and  ${\rm Ru}$ .

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- 5. The method according to claim 2, wherein, in step v), the capacitor lower electrode layer is oxidized by a thickness about  $10\text{\AA}$  to  $800\text{\AA}$ .
- 6. The method according to claim 5, wherein the capacitor lower electrode layer is oxidized by using one process selected from the group consisting of an oxygen plasma treatment process, an ozone plasma treatment process, and an oxygen annealing treatment process.

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7. The method according to claim 6, wherein the oxygen plasma treatment process is carried out with a power of 100W to 30,000W.

- 8 The method according to claim 6, wherein the oxygen plasma treatment process is carried out with a power of 200W to 30,000W.
- 9. The method according to claim 1, wherein the capacitor upper electrode layer is formed by using one selected from the group consisting of TaN, Ta, Ti, TiN and Ru.
- 10. The method according to claim 1, wherein the capacitor lower electrode layer, the dielectric layer, and the upper electrode are formed in-situ.